CLAIMS

What is claimed is:

1. A method of accessing a plurality of memory devices in which a plurality of terminals of a first of the memory devices are interconnected with a corresponding plurality of terminals of a second of the memory devices in a manner that causes the first and second memory devices to function differently responsive to respective address or control signals applied to the interconnected terminals, the method comprising:

if the first memory device is being accessed, applying control or address signals to the interconnected terminals according to a first set of terminal assignments; and

if the second memory device is being accessed, applying control or address signals to the interconnected terminals according to a second set of terminal assignments that is at least in part different from the first set of terminal assignments.

2. The method of claim 1 wherein the parts of the first and second terminal assignments that are different comprise address terminal assignments.

3. The method of claim 1 wherein the parts of the first and second terminal assignments that are different comprise control terminal assignments.

4. The method of claim 1, further comprising applying data signals to the interconnected terminals, and wherein the data signals are applied to the interconnected terminals according to a common set of terminal assignments regardless of whether the first memory device or the second memory device is being accessed

5. The method of claim 1wherein the memory devices comprise dynamic random access memory devices.

6. A method of applying address and control signals to a plurality of identical memory devices in which a plurality of terminals of a first of the memory devices are interconnected with a corresponding plurality of terminals of a second of the memory devices in mirrored configuration, the method comprising:

applying a set of control signals or a set of address signals to the interconnected terminals in a first arrangement if the first memory device is being accessed; and

applying a set of control signals or a set of address signals to the interconnected terminals in a second arrangement if the second memory device is being accessed, the second arrangement being different from the first arrangement.

7. The method of claim 6 wherein the act of applying a set of control signals or a set of address signals to the interconnected terminals in first and second arrangements that are different from each other comprise applying a set of control signals to the interconnected terminals in first and second arrangements that are different from each other.

8. The method of claim 6 wherein the act of applying a set of control signals or a set of address signals to the interconnected terminals in first and second arrangements that are different from each other comprise applying a set of address signals to the interconnected terminals in first and second arrangements that are different from each other.

9. The method of claim 6 wherein the act of applying a set of control signals or a set of address signals to the interconnected terminals in first and

second arrangements that are different from each other comprise applying a set of both address signals and control signals to the interconnected terminals in first and second arrangements that are different from each other.

10. The method of claim 6, further comprising applying data signals to the interconnected terminals in a common arrangement regardless of whether the first memory device is being accessed or the second memory device is being accessed.

11. The method of claim 6 wherein the memory devices comprise dynamic random access memory devices.

12. A method of applying address or control signals to a plurality of identical memory devices mounted on first and second surfaces of memory module substrate in a mirrored configuration so that a plurality of terminals of each of the memory devices mounted on the first surface are interconnected to respective, correspondingly positioned terminals of a respective one of the memory devices mounted on the second surface, the method comprising:

coupling address or control signals to the interconnected terminals for a plurality of the memory devices in a first configuration if the memory devices mounted on the first surface of the substrate are being accessed; and

coupling address or control signals to the interconnected terminals for a plurality of the memory devices in a second configuration that is different from the first configuration if the memory devices mounted on the second surface of the substrate are being accessed.

13. The method of claim 12 wherein the acts of coupling address or control signals to the interconnected terminals in the first or second configuration comprises:

coupling address or control signals to the memory module; and

within the memory module, re-arranging the signals coupled to the memory module to either the first configuration or the second configuration prior to coupling the address or control signals to the interconnected terminals.

14. The method of claim 13 wherein the act of re-arranging the signals coupled to the memory module to either the first configuration or the second configuration comprises re-arranging the signals in a memory hub that is structured to independently access the memory devices.

15. The method of claim 12 wherein the act of coupling address or control signals to the interconnected terminals for a plurality of the memory devices in a first or second configuration comprises coupling address signals to the interconnected terminals in a first or second configuration.

16. The method of claim 12 wherein the act of coupling address or control signals to the interconnected terminals for a plurality of the memory devices in a first or second configuration comprises coupling control signals to the interconnected terminals in a first or second configuration.

17. The method of claim 12, further comprising applying data signals to the interconnected terminals in a common configuration regardless of whether the memory devices being accessed are mounted on the first surface of the substrate or the second surface of the substrate.

18. The method of claim 12 wherein the memory devices comprise dynamic random access memory devices.

19. A memory module, comprising:

an insulative substrate;

a plurality of identical memory devices mounted on first and second opposed surfaces of the insulative substrate, the memory devices being mounted on the substrate in a mirrored configuration so that a plurality of terminals of each of the memory devices mounted on the first surface are interconnected to respective, correspondingly positioned terminals of a respective one of the memory devices mounted on the second surface; and

a memory access device mounted on the substrate, the memory access device having a plurality of terminals that are coupled through the substrate conductors to respective ones of the interconnected terminals, the memory access device being operable to receive a memory request and, in response, to couple address and control signals to the interconnected terminals for a plurality of the memory devices, the address or control signals being coupled to the interconnected terminals in a first configuration if the memory devices mounted on the first surface of the substrate are being accessed, and the address or control signals being coupled to the interconnected terminals in a second configuration that is different from the first configuration if the memory devices mounted on the second surface of the substrate are being accessed.

20. The memory module of claim 19 wherein the memory access device is centrally position on the insulative substrate, and wherein the memory devices are positioned to both sides of the memory access device, the memory access device being operable to couple respective sets of address or control signals in the first or second configuration to the memory devices on each side of the memory access device.

21. The memory module of claim 19 wherein the memory access device comprises a memory hub that is structured to generate the address and control signals to access the memory devices responsive to the memory requests.

22. The memory module of claim 19 wherein the memory hub comprises:

a command queue that is operable to receive the memory requests, the memory queue further being operable to convert the memory requests into respective sets of command and address signals and to output the command and address signals in the order that the respective memory requests were received;

a command scheduler coupled to the command queue to receive the command and address signals from the command queue, the command scheduler arranging the timing of the command and address signals;

a micro command shifter coupled to receive the command and address signals from the command scheduler after the timing of the command and address signals have been arranged, the micro command shifter being operable to output the command and address signals in synchronism with the operation of the memory devices; and

a multiplexer coupled to the micro command shifter to receive the command signals or the address signals from the micro command shifter, the multiplexer being operable to arrange the command or address signals in either the first configuration or the second configuration depending on whether the memory devices on the first surface or the memory devices on the second surface are being accessed, the multiplexer being operable to couple the command or address signals in either the first configuration or the second configuration to the interconnected terminals.

23. The memory module of claim 22, further comprising a ring buffer coupled between the multiplexer and the memory devices.

24. The memory module of claim 19 wherein the memory access device comprises a register that is structured to receive and store address and control

signals forming each of the memory requests, and couple the stored address and control signals to the memory devices.

25. The memory module of claim 19 wherein the memory devices each comprise a dynamic random access memory device.

26. A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a peripheral device port, the system controller further comprising a controller coupled to a system memory port;

at least one input device coupled to the peripheral device port of the system controller;

at least one output device coupled to the peripheral device port of the system controller;

at least one data storage device coupled to the peripheral device port of the system controller; and

a memory module coupled to the system memory port of the system controller, the memory module comprising:

an insulative substrate;

a plurality of identical memory devices mounted on first and second opposed surfaces of the insulative substrate, the memory devices being mounted on the substrate in a mirrored configuration so that a plurality of terminals of each of the memory devices mounted on the first surface are interconnected to respective, correspondingly positioned terminals of a respective one of the memory devices mounted on the second surface; and

a memory access device mounted on the substrate, the memory access device having a plurality of terminals that are coupled through the

substrate conductors to respective ones of the interconnected terminals, the memory access device being coupled to the controller to receive a memory request from the controller and, in response, to couple address and control signals to the interconnected terminals for a plurality of the memory devices, the address or control signals being coupled to the interconnected terminals in a first configuration if the memory devices mounted on the first surface of the substrate are being accessed, and the address or control signals being coupled to the interconnected terminals in a second configuration that is different from the first configuration if the memory devices mounted on the second surface of the substrate are being accessed.

27. The processor-based system of claim 26 wherein the memory access device is centrally position on the insulative substrate, and wherein the memory devices are positioned to both sides of the memory access device, the memory access device being operable to couple respective sets of address or control signals in the first or second configuration to the memory devices on each side of the memory hub.

28. The processor-based system of claim 26 wherein the memory access device comprises a memory hub that is operable to generate the address and command signals in response to a higher level memory request from the controller.

29. The processor-based system of claim 28 wherein the memory hub comprises:

a command queue that is operable to receive the memory requests, the memory queue further being operable to convert the memory requests into respective sets of command and address signals and to output the command and address signals in the order that the respective memory requests were received;

a command scheduler coupled to the command queue to receive the command and address signals from the command queue, the command scheduler arranging the timing of the command and address signals;

a micro command shifter coupled to receive the command and address signals from the command scheduler after the timing of the command and address signals have been arranged, the micro command shifter being operable to output the command and address signals in synchronism with the operation of the memory devices; and

a multiplexer coupled to the micro command shifter to receive the command signals or the address signals from the micro command shifter, the multiplexer being operable to arrange the command or address signals in either the first configuration or the second configuration depending on whether the memory devices on the first surface or the memory devices on the second surface are being accessed, the multiplexer being operable to couple the command or address signals in either the first configuration or the second configuration to the interconnected terminals.

30. The processor-based system of claim 29, further comprising a ring buffer coupled between the multiplexer and the memory devices.

31. The processor-based system of claim 26 wherein the memory devices each comprise a dynamic random access memory device.

32. The processor-based system of claim 26 wherein the memory access device comprises a register that is operable to store the address and command signals received from the controller, and to subsequently couple the stored address and command signals to the memory devices.

33. A processor-based system, comprising:

a processor having a processor bus;

a system controller coupled to the processor bus, the system controller having a peripheral device port and a system memory port;

at least one input device coupled to the peripheral device port of the system controller;

at least one output device coupled to the peripheral device port of the system controller;

at least one data storage device coupled to the peripheral device port of the system controller;

at least one memory module coupled to the system memory port of the system controller, the memory module comprising:

an insulative substrate; and

a plurality of identical memory devices mounted on first and second opposed surfaces of the insulative substrate, the memory devices being mounted on the substrate in a mirrored configuration so that a plurality of terminals of each of the memory devices mounted on the first surface are interconnected to respective, correspondingly positioned terminals of a respective one of the memory devices mounted on the second surface, the interconnected terminals of the at least one memory module being coupled to the to the system memory port of the system controller; and

a memory controller coupled to the system memory port of the system controller, the memory controller being operable to couple address and control signals to the interconnected terminals of the at least one memory module in a first configuration if the memory devices mounted on the first surface of the substrate of the at least one memory module are being accessed, and the address or control signals being coupled to the interconnected terminals of the at least one memory module in a second configuration that is different from the first configuration if the memory devices

mounted on the second surface of the substrate of the at least one memory module are being accessed.

34. The processor-based system of claim 33 wherein the memory controller comprises:

a command queue that is operable to receive the memory requests, the memory queue further being operable to convert the memory requests into respective sets of command and address signals and to output the command and address signals in the order that the respective memory requests were received;

a command scheduler coupled to the command queue to receive the command and address signals from the command queue, the command scheduler arranging the timing of the command and address signals;

a micro command shifter coupled to receive the command and address signals from the command scheduler after the timing of the command and address signals have been arranged, the micro command shifter being operable to output the command and address signals in synchronism with the operation of the memory devices; and

a multiplexer coupled to the micro command shifter to receive the command signals or the address signals from the micro command shifter, the multiplexer being operable to arrange the command or address signals in either the first configuration or the second configuration depending on whether the memory devices on the first surface or the memory devices on the second surface are being accessed, the multiplexer being operable to couple the command or address signals in either the first configuration or the second configuration to the interconnected terminals of the at least one memory module.

35. The processor-based system of claim 34, further comprising a ring buffer coupled between the multiplexer and the interconnected terminals of the memory devices.

36. The processor-based system of claim 33 wherein the memory devices each comprise a dynamic random access memory device.

37. A memory hub having an input port and a plurality of output terminals, the memory hub being responsive to a memory request received at the input port to couple address and control signals to the output terminals, the address or control signals being coupled to the output terminals in a first configuration if the memory request is directed to a first memory device, the address or control signals being coupled to the output terminals in a second configuration if the memory request is directed to a second memory device, the second configuration being different from the first configuration.

38. The memory hub of claim 37 wherein the memory hub comprises:

a command queue that is operable to receive the memory requests, the memory queue further being operable to convert the memory requests into respective sets of command and address signals and to output the command and address signals in the order that the respective memory requests were received;

a command scheduler coupled to the command queue to receive the command and address signals from the command queue, the command scheduler arranging the timing of the command and address signals;

a micro command shifter coupled to receive the command and address signals from the command scheduler after the timing of the command and address signals have been arranged, the micro command shifter being operable to output the

command and address signals in synchronism with the operation of the memory devices; and

a multiplexer coupled to the micro command shifter to receive the command signals or the address signals from the micro command shifter, the multiplexer being operable to arrange the command or address signals in either the first configuration or the second configuration depending on whether the memory devices on the first surface or the memory devices on the second surface are being accessed, the multiplexer being operable to couple the command or address signals in either the first configuration or the second configuration to the interconnected terminals.

39. The memory hub of claim 38, further comprising a ring buffer coupled between the multiplexer and the memory devices.

40. The memory hub of claim 37 wherein the command and address signals generated by the memory hub comprise dynamic random access memory command and address signals.